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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,273	03/31/2004	Hiroaki Jo	118429	5405
25944 7590 05/31/2007 OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			EXAMINER ZUBAJLO, JENNIFER L	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/813,273

Applicant(s)

JO, HIROAKI

Examiner

Jennifer Zubajlo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status3/31/04

- 1) ☒ Responsive to communication(s) filed on 5/24/2007.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 3/31/04 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All, b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>3/31/2004 and 12/22/2006</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3 and 5-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Mutsumi Kimura (Patent No.: US 6,518,962 B2), hereinafter Kimura et al.

3. For claim 1, Kimura et al. teaches:

A pixel circuit disposed at the intersection of a scanning line and a data line (signal line) (see figures 1, 2, 11-17, and 19 – lines 131 and 132), comprising: a capacitor (figures 11-17 and 19 – element 222) that accumulates, when the scanning line is selected, charge in accordance with current flowing through the data line or voltage on the data line; a drive transistor (figures 11-17 and 19 - item 223) being turned ON/OFF in accordance with the charge accumulated in the capacitor, the drive transistor allowing current to flow between a first terminal and a second terminal of the drive transistor (see figures 11-17 and 19 – terminals are on both sides of transistor 223); a driven element having one end that is electrically connected to the first terminal, the driven element being driven at least by the current allowed to flow by the drive transistor (see figures 11-17 and 19 – device 224) ; a detector that detects voltage at the one end of the driven element (see figure 15 (241), 16 (242), 19 (104, 110, 204, 16") – note by

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detecting emitted light voltage is also detected) ; and a correction circuit that corrects the current flowing through the driven element in accordance with the absolute value of the voltage detected by the detector (see figures 17 and 19 - correction circuit 209).

As to claim 2 (dependent on claim 1), note figure 19 teaches the correction circuit (209) generating current in accordance with the voltage detected by the detector (204) and adding the generated current to the current allowed to flow by the drive transistor (223).

As to claim 3 (dependent on claim 2), note figures 11-14 (transistors 231-234), and 19 teach the detector being a detection transistor having a gate that is connected to the one end of the driven element, the detection transistor being turned ON/OFF in accordance with the gate voltage thereof, and the detection transistor allowing current to flow between a third terminal and a fourth terminal thereof, and the correction circuit generating current associated with current flowing between a first terminal and a second terminal of the detection transistor.

As to claim 5 (dependent on claim 2), note figure 19 teaches the correction circuit (209) inverting and amplifying the voltage detected by the detector (204) and applying the inverted, amplified voltage to the driven element.

As to claim 6 (dependent on claim 2), note figures 11-17 and 19 teach a switch (221) having one end that is connected to the first terminal and having another end that is connected to the one end of the driven element, the switch controlling a connection between the drive transistor (223) and the driven element when the scanning line (131) is unselected, the detector (104, 204, 16") detecting voltage at the one end of the

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switch, and the correction circuit (209) allowing the generated current to flow through the one end of the switch.

As to claim 7 (dependent on claim 1), note figures 11-17 and 19 teach a switching transistor (221) being turned ON when the scanning line (131) is selected; and a compensation transistor for diode-connecting (241, 242, 110) the drive transistor (223) when the scanning line is selected, the capacitor (222) accumulating, when the switching transistor is turned ON, the charge in accordance with the current flowing through the data line (132).

As to claim 8 (dependent on claim 1), note figures 11-17 and 19 teach a switching transistor (221) being turned ON when the scanning line (131) is selected, the capacitor (222) accumulating, when the switching transistor is turned ON, the charge in accordance with the voltage on the data line (132).

As to claim 9 (dependent on claim 1), note figures 15, 16, and 19 teach the correction circuit (209) adjusting, when the absolute value of the voltage detected by the detector (104, 204, 16") is large, voltage between the first terminal or the second terminal of the drive transistor (223) and the other end of the driven element (241, 242, 110) by increasing the voltage in terms of absolute value.

For claim 10, Kimura et al. teaches:

A pixel circuit (see figure 19 element 115) comprising: a drive transistor (see figure 19 element 223) having a gate that is connected to one end of a capacitor (see figure 19 element 222), and a connection between a first terminal and a second terminal of the

drive transistor being set in accordance with charge accumulated in the capacitor; a driven element (see figure 19 element 110) having one end that is electrically connected to the first terminal (see figure 19 – source end of transistor 223); a detector that detects voltage at the one end of the driven element (see figure 19 element 204 - note by detecting emitted light voltage is also detected); and a correction circuit (see figure 19 element 209) including an input end to receive a signal indicating the voltage detected by the detector and an output end electrically connected to the first terminal, the correction circuit supplying current in accordance with the absolute value of the voltage indicated by the signal input to the input end to the output end (see figure 19 elements 204, 16", 207, 209).

As to claim 11 (dependent on claim 10), note figures 11-17 and 19 teach the detector being a detection transistor (231-234) having a gate that is connected to said one end of the driven element, and the connection between a third terminal and a fourth terminal of the detection transistor being set in accordance with the gate voltage thereof.

As to claim 12 (dependent on claim 11), note figures 11-17 and 19 teach the correction circuit (209) including a first transistor having a fifth terminal that is connected to the gate, a sixth terminal that is connected to a power-supply-voltage (133) feed line, and the fifth terminal being connected to the third terminal; and a second transistor having a gate that is connected to the gate of the first transistor and the fifth terminal, a seventh terminal that is electrically connected to the first terminal, and an eighth terminal that is connected to the feed line.

As to claim 13 (dependent on claim 11), note figures 11-17 and 19 teach the correction circuit including: a third transistor, a reference voltage being applied to the gate thereof, a ninth terminal thereof that is connected to the third terminal, and a tenth terminal that is connected to a power-supply-voltage feed line; and a fourth transistor having a gate that is connected to the ninth terminal, an eleventh terminal that is electrically connected to the first terminal, and a twelfth terminal that is connected to the feed line.

As to claim 14 (dependent on claim 10), note figures 11-17 and 19 teach a switch (221) having one end that is connected to the first terminal, and having another end that is connected to said one end of the driven element, the detector (104, 204, 16") detecting voltage at said one end of the switch.

As to claim 15 (dependent on claim 10), note figures 13, 14, and 19 teach a compensation transistor (233, 234) that short-circuits between the gate of the drive transistor (223) and the first terminal, the capacitor (222) accumulating charge in accordance with the voltage at the first terminal when the compensation transistor short-circuits between the gate of the drive transistor and the first terminal.

For claim 16, Kimura et al. teaches:

An electro-optical device, comprising: a plurality of data lines (figure 1 element 132 and column 20 lines 9-13); a plurality of scanning lines (figure 1 element 132 and column 20 lines 9-13); and a plurality of pixel circuits (see figures 1 and 19 element 10) as set forth in claim 1 (see above rejection of claim 1), the pixel circuits being disposed at the

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intersections of the plural data lines and the plural scanning lines (see figure 1 element 10).

For claim 17, Kimura et al. teaches:

An electro-optical device, comprising: pixel circuits disposed at intersections of a plurality of scanning lines and a plurality of data lines (see figure 1 (10, 131, 132) and column 20 lines 9-13), the pixel circuits including driven elements (see figure 19 elements 10, 110, 115); a scanning-line drive circuit (see figure 19 element 11) that selects the scanning lines (131) one at a time; and a data-line drive circuit (see figure 19 element 12) that supplies, when the scanning line is selected by the scanning-line drive circuit, current that is to flow through the driven element of each corresponding pixel circuit associated with the scanning line or voltage associated with the current via each corresponding data line, each of the pixel circuits including: a capacitor (see figure 19 element 222) that accumulates, when the corresponding scanning line is selected, charge in accordance with current flowing through the corresponding data line or voltage on the corresponding data line; a drive transistor (see figure 19 element 223) being turned ON/OFF in accordance with the charge accumulated in the capacitor, the drive transistor allowing current to flow between a first terminal and a second terminal (see figure 19 – source and drain of transistor 223) of the drive transistor; a driven element having one end that is electrically connected to the first terminal (see figure 19 elements 110 and 115), the driven element being driven by at least the current allowed to flow by the drive transistor; a detector (see figure 19 elements 204 and 16”) that

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detects voltage at the one end of the driven element; and a correction circuit (see figure 19 element 209) that corrects the current flowing through the driven element in accordance with the absolute value of the voltage detected by the detector.

For claim 18, Kimura et al. teaches:

An electronic apparatus, comprising: an electro-optical device as set forth in claim 16 (see above rejection of claims 1 and 16).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mutsumi Kimura (Patent No.: US 6,518,962 B2), hereinafter Kimura et al.

As to claim 4 (dependent on claim 3), Kimura et al. teaches the limitations as described above in claims 1-3.

Kimura et al. does not directly teach the correction circuit being a current mirror circuit that generates a mirror current of the current flowing between the third terminal and the fourth terminal.

However, it is well known that a current mirror is a circuit designed to copy a current. An ideal current mirror is an ideal current amplifier. Therefore in correction to prevent a degraded image, a constant current needs to flow through the organic EL elements and over time the current flowing is reduced therefore in correction this current needs to increase and it would be obvious to do so with the use of a current mirror.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kimura with the well known current mirror for correction of current flowing through the organic EL elements in order to emit light with sufficient brightness to keep the image quality from degrading.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patent Numbers: US 6,462,722 B1, US 6,812,651 B2, and US 6,650,060 B2.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer Zubajlo whose telephone number is (571) 270-1551. The examiner can normally be reached on Monday-Friday, 8 am - 5 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jennifer Zubajlo



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SUPERVISORY PATENT EXAMINER